IN THE CLAIMS:

Please amend the claims as follows:

1. (currently amended) A circuit to encode binary digital signals so as to reduce EMI emissions during signal transmission across a bus or interconnect comprising:

circuitry to generate a pseudo-random pattern of binary digital signals; and

circuitry to apply logic operations to selected binary digital signals, the selected binary digital signals to be encoded prior to signal transmission across the bus or interconnect, with selected binary digital signals of the pseudo-random pattern in order to reduce the harmonic content of the selected binary digital signals to be encoded;

wherein the binary digital signals comprise regular binary digital signals and wherein the bus or interconnect includes at least two distinct selected binary digital signals to be encoded.

2. (original) The circuit of claim 1, wherein the logic operations comprise one of a logical exclusive OR operation and a logical exclusive NOR operation.

3. (canceled).

4. (currently amended) The circuit of claim 1, wherein the regular binary digital signals comprise ~~video~~ at least twenty four digital video interface signals.

5. (previously amended) The circuit of claim 1, wherein the regular binary digital signals comprise digital clock signals.

6. (currently amended) The circuit of claim 1, wherein the circuitry to generate a pseudo-random pattern of binary digital signals comprises more than one

pseudo-random pattern generator to generate more than one pseudo-random pattern; and wherein the circuitry to apply logic operations comprises circuitry to apply logic operations to selected binary digital signals, the selected binary digital signals to be encoded prior to signal transmission across the bus or interconnect, with selected binary digital signals of the more than one pseudo-random patterns in order to reduce the harmonic content of the selected binary digital signals to be encoded.

7. (original) The circuit of claim 1, wherein said circuit is embodied on a motherboard.

8. (original) The circuit of claim 1, wherein said motherboard is embodied in a personal computer.

9. (currently amended) A method of encoding binary digital signals so as to reduce EMI emissions during signal transmission across a bus or interconnect comprising:

generating a pseudo-random pattern of binary digital signals;

applying logic operations to selected binary digital signals, the selected binary digital signals to be encoded prior to signal transmission across the bus or interconnect, with selected binary digital signals of the pseudo-random pattern in order to reduce the harmonic content of the selected binary digital signals to be encoded;

wherein the binary digital signals comprise regular binary digital signals and wherein the bus or interconnect includes at least two distinct selected binary digital signals to be encoded.

10. (original) The method of claim 9, wherein the logic operations comprise one of a logical exclusive OR operation and a logical exclusive NOR operation.

11. (canceled).

12. (currently amended) The method of claim 9, wherein the regular binary digital signals comprise ~~video~~ at least twenty four digital video interface signals.

13. (previously amended) The method of claim 9, wherein the regular binary digital signals comprise digital clock signals.

14. (currently amended) The method of claim 9, wherein generating a pseudo-random pattern of binary digital signals comprises generating more than one pseudo-random pattern; and wherein applying logic operations comprises applying logic operations to selected binary digital signals, the selected binary digital signals to be encoded prior to signal transmission across the bus or interconnect, with selected binary digital signals of the more than one pseudo-random patterns in order to reduce the harmonic content of the selected binary digital signals to be encoded.

15. (currently amended) A circuit to decode binary digital signals that have been encoded so as to reduce EMI emissions during signal transmission across a bus or interconnect comprising:

circuitry to apply logic operations to selected encoded binary digital signals to be decoded, the encoded binary digital signals being encoded to reduce the harmonic content of the pre-encoded binary digital signals, with selected binary digital signals of a pseudo-random pattern used to encode the encoded binary digital signals;

wherein the binary digital signals comprise regular binary digital signals and wherein the bus or interconnect includes at least two distinct selected binary digital signals to be encoded.

16. (previously amended) The circuit of claim 15, wherein the logic operations comprise one of a logical exclusive OR operation and a logical exclusive NOR operation.

17-19 (canceled).

20. (original) The circuit of claim 15, wherein the circuitry to apply logic operations includes circuitry to generate a pseudo-random pattern of binary digital signals.

21. (currently amended) The circuit of claim 20, wherein the circuitry to generate a pseudo-random pattern of binary digital signals comprises more than one pseudo-random pattern generator to generate more than one pseudo-random pattern; and wherein the circuitry to apply logic operations comprises circuitry to apply logic operations to selected binary digital signals, the selected binary digital signals to be encoded prior to signal transmission across the bus or interconnect, with selected binary digital signals of the more than one pseudo-random patterns in order to reduce the harmonic content of the selected binary digital signals to be encoded.

22. (original) The circuit of claim 15, wherein said circuit is embodied on a motherboard.

23. (original) The circuit of claim 15, wherein said motherboard is embodied in a personal computer.

24. (currently amended) A method of decoding binary digital signals that have been encoded so as to reduce EMI emissions during signal transmission across a bus or interconnect comprising:

applying logic operations to selected encoded binary digital signals to be decoded, the encoded binary digital signals being encoded to reduce the harmonic content of the pre-encoded binary digital signals, with selected binary digital signals of a pseudo-random pattern used to encode the encoded binary digital signals;

wherein the binary digital signals comprise regular binary digital signals and wherein the bus or interconnect includes at least two distinct selected binary digital signals to be encoded.

25. (original) The method of claim 24, wherein the logic operations comprise one of a logical exclusive OR operation and a logical exclusive NOR operation.

26. (original) The method of claim 24, and further comprising, generating a pseudo-random pattern of binary digital signals.

27. (currently amended) The method of claim wherein generating a pseudo-random pattern of binary digital signals comprises generating more than one pseudo-random pattern of binary digital signals; and wherein applying logic operations comprises applying logic operations to selected binary digital signals, the selected binary digital signals to be encoded prior to signal transmission across the bus or interconnect, with selected binary digital signals of the more than one pseudo-random patterns in order to reduce the harmonic content of the selected binary digital signals to be encoded.

28. (currently amended) A circuit to encode binary digital signals so as to reduce EMI emissions during signal transmission across a bus or interconnect comprising:

circuitry to apply at least one pseudo-random pattern of binary digital signals to encode selected binary digital signals so as to reduce the harmonic content of the selected binary digital signals;

wherein the binary digital signals comprise regular binary digital signals and wherein the bus or interconnect includes at least two distinct selected binary digital signals to be encoded.

29. (canceled).

30. (currently amended) The circuit of claim 28, wherein the regular binary digital signals comprise ~~video~~ at least twenty four digital video interface signals.

31. (previously amended) The circuit of claim 28, wherein the regular binary digital signals comprise digital clock signals.

32. (original) The circuit of claim 28, wherein said circuit is embodied on a motherboard.

33. (original) The circuit of claim 28, wherein said motherboard is embodied in a personal computer.

34. (currently amended) A method of encoding binary digital signals so as to reduce EMI emissions during signal transmission across a bus or interconnect comprising:

applying at least one pseudo-random pattern of binary digital signals to encode selected binary digital signals so as to reduce the harmonic content of the selected binary digital signals;

wherein the binary digital signals comprise regular binary digital signals and wherein the bus or interconnect includes at least two distinct selected binary digital signals to be encoded.

35. (canceled).

36. (currently amended) The method of claim 34, wherein the regular binary digital signals comprise ~~video~~ at least twenty four digital video interface signals.

37. (previously amended) The method of claim 34, wherein the regular binary digital signals comprise digital clock signals.

38. (newly added) The method of claim 34, further comprising:

transmitting the pseudo-random pattern of binary digital signals across the across the bus or interconnect along with the encoded binary digital signals.

39. (newly added) The method of claim 38, further comprising:

synchronizing the transmission of the encoded binary digital signals with the transmission of the pseudo-random pattern of binary digital signals.

40. (newly added) The circuit of claim 1, further comprising:

circuitry to transmit the pseudo-random pattern of binary digital signals across the bus or interconnect along with the encoded binary digital signals.

41. (newly added) The circuit of claim 40, further comprising:

delay circuitry to synchronize transmission of the encoded binary digital signals with the transmission of the pseudo-random pattern of binary digital signals.

42. (newly added) The method of claim 9, further comprising:

transmitting the pseudo-random pattern of binary digital signals across the across the bus or interconnect along with the encoded binary digital signals.

43. (newly added) The method of claim 42, further comprising:

synchronizing the transmission of the encoded binary digital signals with the transmission of the pseudo-random pattern of binary digital signals.

44. (newly added) The circuit of claim 28, further comprising:

circuitry to transmit the pseudo-random pattern of binary digital signals across the bus or interconnect along with the encoded binary digital signals.

45. (newly added) The circuit of claim 44, further comprising:

delay circuitry to synchronize transmission of the encoded binary digital signals with the transmission of the pseudo-random pattern of binary digital signals.